IN THE CLAIMS

1-22 (Cancelled).

23. (Previously Presented) A graphics chip having an embedded DRAM, the chip comprising:

an embedded DRAM partitioned into a plurality of embedded drawing buffers;

a drawing engine to concurrently access the embedded drawing buffers for rendered drawing information, the drawing engine to implement concurrent drawing processes, and the drawing processes interrelated in a predetermined manner;

a plurality of independent read FIFO buffers and write FIFO buffers used by the concurrent drawing processes to access the embedded drawing buffers; and

an access priority engine to communicate with substantially all FIFO buffers needing access to a given embedded drawing buffer, and grant access priority in a dynamic manner to each of such FIFO buffers serially.

24. (Previously Presented) The graphics chip of claim 23, further including a wide bandwidth access bus to connect a FIFO buffer having access priority with the embedded DRAM.

25. (Previously Presented) The graphics chip of claim 23, wherein each FIFO buffer has its own address register and offset register permitting each FIFO buffer to access the entire address space of the embedded DRAM.

26. (Previously Presented) A graphics chip having an embedded DRAM buffer, the chip comprising:

an embedded DRAM partitioned into a plurality of embedded drawing buffers;

a drawing engine to concurrently access the embedded drawing buffers for rendered drawing Information, the drawing engine to implement concurrent drawing processes, and the drawing processes interrelated in a predetermined manner;

a plurality of independent read FIFO buffers and write FIFO buffers used by the concurrent drawing processes to access the embedded drawing buffers; and

wherein the embedded DRAM is arranged in at least two independent memory banks, each of the memory banks includes a separate wide bandwidth access bus, and each wide bandwidth access bus includes a corresponding access priority engine communicating with at least one of the read and write FIFO buffers.

27. (Previously Presented) The graphics chip of claim 26, further comprising a plurality of programmable switches, each FIFO buffer connectable to a selected access bus and a corresponding access priority engine via the programmable switches.

28. (Previously Presented) The graphics chip of claim 27, further comprising at least two embedded drawing buffers located within a single memory bank of the embedded DRAM, and the FIFO buffers for the corresponding drawing processes connected to the access bus and the priority engine for the memory bank via the programmable switches.

29. (Previously Presented) The graphics chip of claim 27, further comprising means

permitting a host device to program the switches for configuring the drawing processes via FIFO buffers to access drawing buffers in selected memory banks.